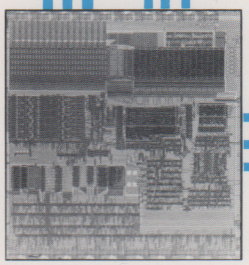
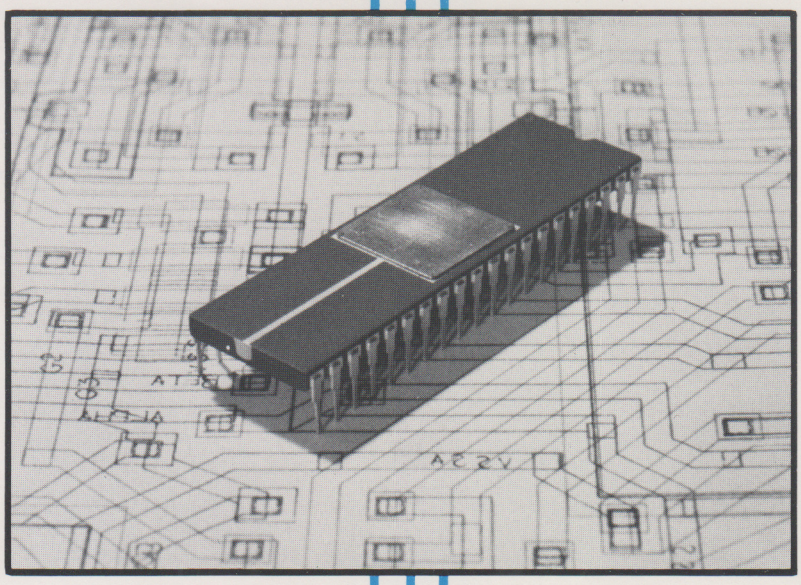
MAC-4





SPECIFICATION SHEET

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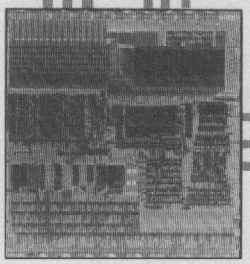
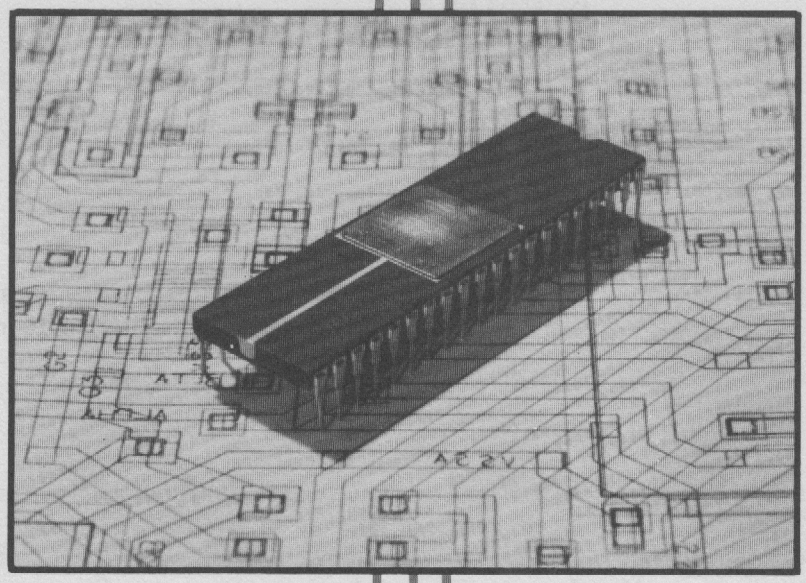
MAC-4





SPECIFICATION SHEET

PRELIMINARY DATA SHEET: Specifications are not final and will be subject to change without notice

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NOTICE

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Bell Laboratories

November 1978

MAC-4
SINGLE-CHIP MICROCOMPUTER

- ☐ CPU, ROM, RAM, I/O In a Single 40-Pin Package
- ☐ Powerful Bit-Oriented Instruction Set
- ☐ 4 Source And 4 Destination Addressing Modes
- ☐ 4,8,12,16 Bit Operations
- ☐ DC To 3.58 MHz (TV Crystal) Clock
- ☐ Low Current Drain and Unregulated Single Supply for MOS Compatibility
- ☐ Split Power Supply for TTL Compatibility
- ☐ 2 Standard Memory Options:
  1280x4 or 2Kx4 ROM
  80x4 or 128x4 RAM
- ☐ 34 I/O Lines Include:
  16 Programmable I/O Latches
  8 Bit I/O Port
  4 Bit Input Port
  One Level Interrupt
- ☐ Serial/Parallel Direct Memory Access (DMA) Operations
- ☐ 12 Bit Event Counter
- ☐ User PLA

The MAC-4 is a one-chip, totally self-contained microcomputer primarily designed for controller system applications. It is implemented in CMOS technology for low power dissipation, an asset for telephone loop power applications. Two power pins (V_{DD} and V_{CC}), are supplied for optimization of both I/O interfacing and speed-power tradeoffs. They may be tied together and range from 3.5 to 10 volts. When V_{CC} is 5V, all data I/O are TTL compatible. Maximum operating frequency is achieved when V_{DD} is 10V.

The device features a versatile CPU and contains ROM program memory, RAM data memory, on-chip oscillator and clock circuits, and a flexible I/O structure. Two standard memory options are available: 1280x4 ROM and 80x4 RAM; or 2Kx4 ROM and 128x4 RAM. The memory can be expanded on a custom basis to 3840x4 ROM and 192x4 RAM. Additionally, its I/O features include 16 programmable I/O latches, a 32-term User PLA, an 8-bit I/O port, a 12-bit event counter, serial and parallel DMA, and one level of interrupt.

The MAC-4 has a rich instruction set designed for program memory efficiency and extensive bit handling capability. It features four source and four destination addressing modes that include autoload and autoincrement capabilities. Additionally, variable width operands (4,8,12,16 bits) can be processed by most instructions.

To provide maximum flexibility for production testing, prototyping, and preproduction systems, an External Memory Access ($\overline{EMA}$) mode is available. The final version of the program can then be masked into on-chip ROM memory. A MAC-4 prototyping module, PROMAC, is available to assist the user in software development. A MAC-4 development system, MAC-MATE will also be available.

For further information, call MH extension 4630, 4599 or HO 6228.

ABSOLUTE MAXIMUM RATINGS

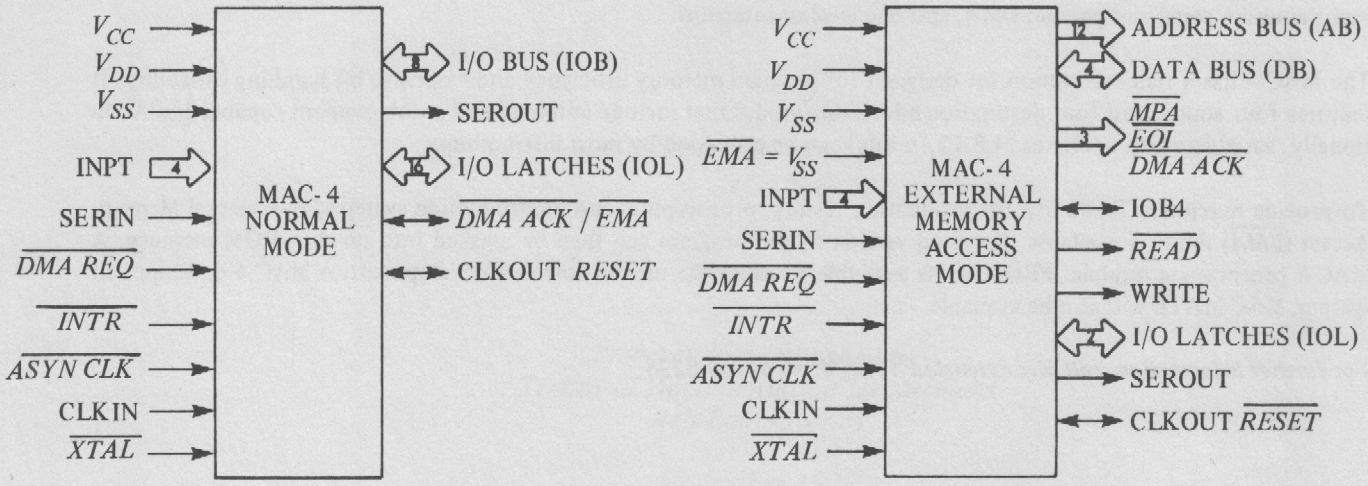
Ambient Temperature . . . . . −40°C to +85°C
Storage Temperature . . . . . −40°C to +85°C
D.C. Supply Voltage . . . . . V_{SS} −0.5V to V_{SS} + 12V
Input Voltage . . . . . V_{SS} −0.5V to V_{DD} + 0.5V, V_{CC} + 0.5V
Power Dissipation per package 500mW

OPERATING CONDITIONS T_A = −40°C to 85°C, V_{SS} = 0V

Parameter	Conditions		Limits		Remarks
	V_{CC}	V_{DD}	Min	Max	
Supply Voltage (V) (See Note)					CAUTION: In all cases, $V_{DD} \geqslant V_{CC}$
V_{CC} V_{DD}			3.5V	10V	
V_{CC} (TTL)			4.5V	5.5V	Typical = 5V, for TTL compatibility
Input Voltage Range			V_{SS}	to V_{CC}	
Input Clock Frequency (MHz)	3.5V	3.5V	DC	0.2	Provisional
	5V	5V	DC	1.5	
	5/9V	9V	DC	3.58	
Clock Out Pulse Width (ns)	3.5V	3.5V	5000		Provisional
	5V	5V	670		
	5/9V	9V	280		

Note: Maximum specified operating frequency occurs when V_{DD} is 9V ± 1V. CAUTION: to prevent possible damage to the device ensure that $V_{DD} \geqslant V_{CC}$ at all times.

FUNCTIONAL SYMBOLS



D.C. CHARACTERISTICS $T_A = -40°C$ to $85°C$, $V_{SS} = 0V$

Symbol	Parameter	Conditions (V) (See Note 1)		Limits		Unit	Remarks
		V_{CC}	V_{DD}	Min	Max		
V_{IL}	Input Voltage Low	–	–		0.2 V_{CC}	V	CMOS compatible
		4.5	10.0		0.8	V	TTL compatible
V_{IH}	Input Voltage High	–	–	0.8 V_{CC}		V	CMOS compatible
		5.5	10.0	1.8		V	$I_{IH_{MAX}} = -100\ \mu A$ (See Note 2)
V_{OL}	Output Voltage Low	–	–		0.05	V	$I_{OL} = 0$, CMOS compatible
		4.5	4.5		0.4	V	$I_{OL} = 0.8$mA TTL compatible
		4.5	8.0		0.4	V	$I_{OL} = 0.8$mA TTL compatible
V_{OH}	Output Voltage High	–	–	V_{CC} –0.05		V	CMOS compatible
		4.5	8.0	2.4		V	$I_{OH} = -100\ \mu A$ TTL compatible
I_{OL}	Output Sink Current	4.5	4.5	0.8		mA	$V_{OL} = 0.4V$
		4.5	8.0	0.8		mA	$V_{OL} = 0.4V$
I_{OH}	Output Source Current	3.5	3.5				
		4.5	8.0	50		μA	$V_{OH} = 2.4V$ min
		9.0	9.0				
I_{IL}	Input Leakage Current Low (per pin)	–	–		–100	nA	$V_{IH} = V_{DD}$, (See Note 3)
I_{IH}	Input Leakage Current High (per pin)				100	nA	
I_{DD}	V_{DD} Supply Current					mA	
I_{CC}	V_{CC} Supply Current					mA	
P_D	Power Dissipation	3.5	3.5		10	mW	f = 200 kHz (provisional)
		5.0	9.0		200	mW	f = 3.58 MHz

Notes:

1. See Note given in Operating Conditions.
2. On-Chip mask programmable pull-up resistors enable $V_{III} = 1.8V$ for TTL compatibility, provided the driver gate OFF-stage leakage current ($I_{III_{MAX}}$) conditions are satisfied.
3. Without pull-up resistors at I/O latches (IOL). Conditions are MAC-4 in HALT and normal modes, and I/O latches set to HIGH.

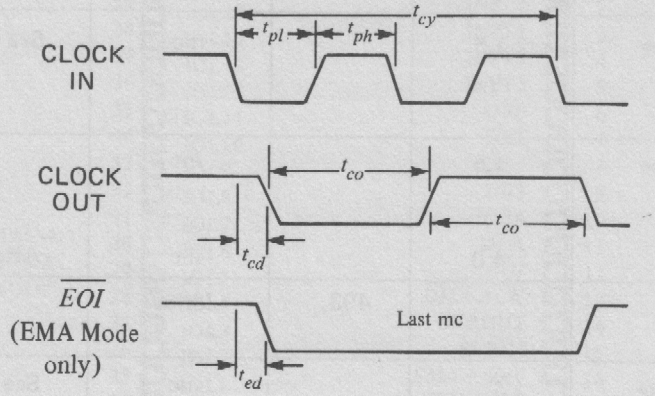
TIMING CHARACTERISTICS

$T_A = -40°C$ to $85°C$, $V_{DD} = 9V \pm 1V$, $V_{CC} = 5V \pm 0.5V$, $V_{SS} = 0V$

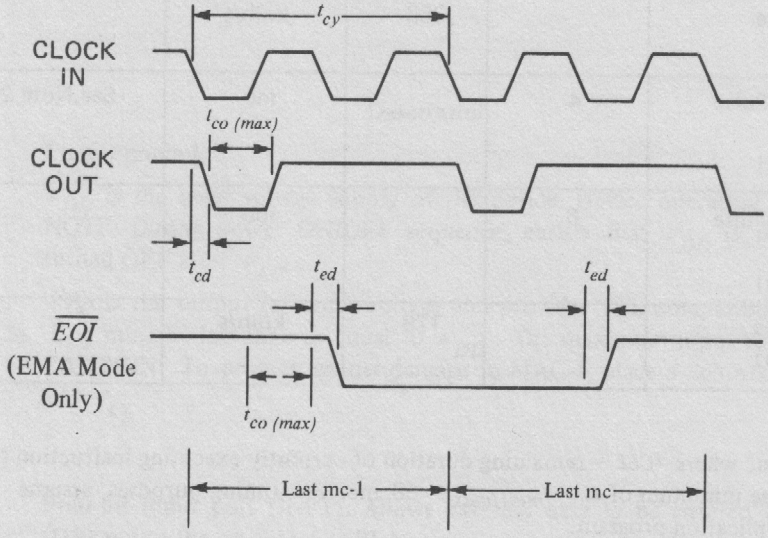
Symbol	Parameter	Limits		Units	Remarks
		Min	Max		
t_{cy}	Machine Cycle Time	560		ns	
t_{pl}	Clock In Low	140			
t_{ph}	Clock In High	140			
t_{co}	Clock Out Pulse Width	280	4000	ns	f (V_{DD}), max. value at slow clock @ $V_{DD} = 3.5V$.
t_{cd}	Clock Out Delay	80		ns	f (V_{DD}), max. at $V_{DD} = 3.5V$ min. at $V_{DD} = 9V$
t_{ed}	$\overline{EOI}$ Delay				
t_{ip}	Interrupt Pulse Width	1	3	mc	mc = machine cycle
t_{ECP}	Interval between Event Counter Pulses	58		mc	Worst case min. (See Note 1)
t_{ECW}	Event Counter Pulse Width	1		mc	
f_{EC}	Event Counter Frequency		30.8	kHz	@ 3.58 MHz, and assuming t_{ECP} (min.)|max.
	DMA Operations				
	DMA In:				
t_{DML}	Latency Time	4	54	mc	t_{CEI} + 4 mc
		12		mc	Worst case min.
t_{DME}	End Response				
	DMA Out:				
t_{DML}	Latency Time	6	56	mc	t_{CEI} + 6 mc
		14			Worst case min.
t_{DME}	End Response				
t_{ace}	$\overline{ASYN\ CLK}$ End Delay	0		ns	
t_{acl}	$\overline{ASYN\ CLK}$ Pulse Width Low (Serial In)	1		mc	See Note 2
t_{ach}	$\overline{ASYN\ CLK}$ Pulse Width High (Serial In)	1		mc	
	Transfer Rate (Serial In)		895	k bits/s	7 bits serial is allowed during DMA latency

WAVEFORMS

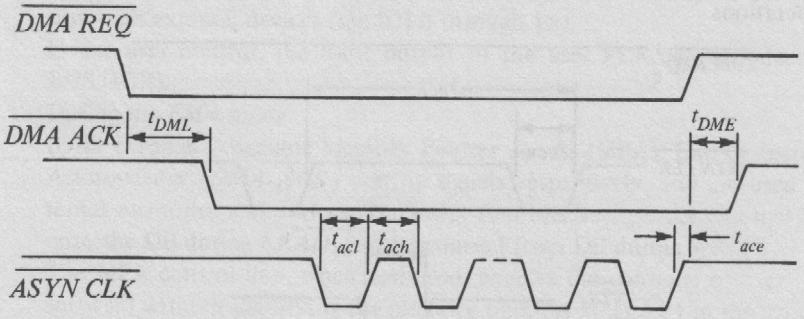
A. Normal Clock (140 ns ≤ tp ≤ 2 μs)



B. Slow Clock (tp > 2 μs)



C. DMA Operations



TIMING CHARACTERISTICS (Cont.)

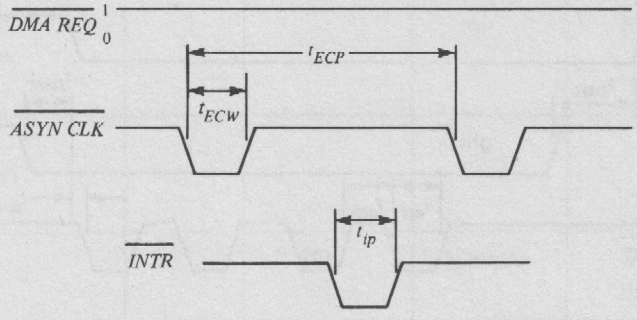
Symbol	Parameter	Limits		Units	Remarks
		Min	Max		
t_{acl}	$\overline{ASYN\ CLK}$ Pulse Width Low (Serial Out)	1.5		mc	See Note 2.
t_{ach}	$\overline{ASYN\ CLK}$ Pulse Width High (Serial Out)	1.5 4.0		mc mc	After each 4-bit string.
	Transfer Rate (Serial Out)		493	kbits/s	
t_{acl}	$\overline{ASYN\ CLK}$ Pulse Width Low (Parallel In)	1		mc	See Note 2.
t_{ach}	$\overline{ASYN\ CLK}$ Pulse Width High (Parallel In)	4		mc	
	Transfer Rate (Parallel In)		358	knib/s	
t_{acl}	$\overline{ASYN\ CLK}$ Pulse Width Low (Parallel Out)	4		mc	See Note 2.
t_{ach}	$\overline{ASYN\ CLK}$ Pulse Width High (Parallel Out)	6		mc	
	Transfer Rate (Parallel Out)		179	knib/s	

Notes:

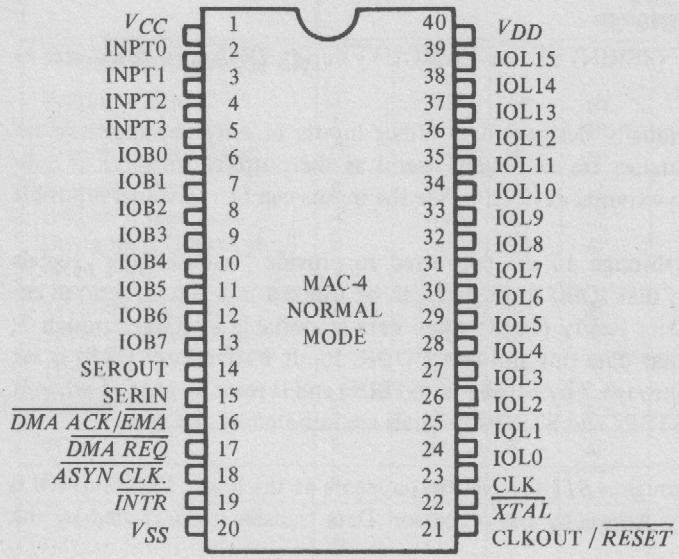
1. $t_{ECP(MIN)} = t_{CEI} + 8$ mc where t_{CEI} = remaining duration of currently executing instruction (maximum t_{CEI} possible = 50 mc). Worst case minimum of $t_{ECP(min)/max} = 58$ mc. For timing purposes, assume t_{CEI} = duration of longest instruction in application program.
2. If these minimum asynchronous clock ($\overline{ASYN\ CLK}$) pulse widths are not maintained, erroneous data transfers may result.

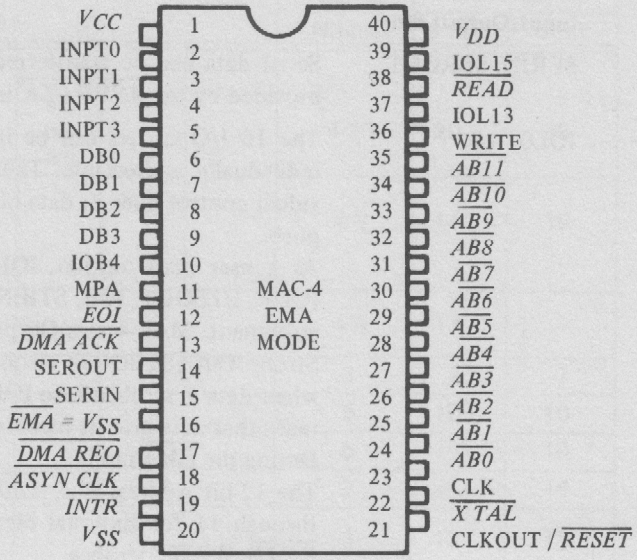
WAVEFORMS (Cont.)

D. Event Counter Operations



STANDARD PIN CONFIGURATION





MAC-4 PIN DESCRIPTION

Power Supply Pins	Description
V_{SS}	Circuit ground.
V_{DD}	V_{DD} is the main voltage supply of the device. Device operating speed will vary with V_{DD} NOTE: During power ON/OFF sequence, ensure that V_{DD} is turned ON before V_{CC} and turned OFF after V_{CC}.
V_{CC}	V_{CC} is the output reference voltage and provides TTL compatibility at 5V IN ALL CASES, V_{CC} must be less than or equal to V_{DD}. The maximum input voltage swing is V_{SS} to V_{CC}. CAUTION: To protect against damage to MAC-4, place a Schottky diode between pins V_{DD} and V_{CC}.
Input/Output Pins	
INPT0 - 3	Four-bit input port (INPT). Allows external data to be entered onto the internal Data Bus (DB) and to the on-chip user PLA. Additionally, it can be used to input parallel data during DMA operations.
IOB0 - 7	Two 4-bit bidirectional ports which can be written to or read from directly by the DB. The ports are statically latched for both inputs and outputs, thus providing an 8-bit bidirectional port for easy interfacing to an 8-bit environment. Moreover, through a mask option, four "handshaking" signals are provided in lieu of four I/O latches for data transfer synchronization with external devices (see IOL0 through 15). Under user control, the 8-bit output of the user PLA can be selected to appear at the I/O BUS (IOB). During the EMA mode: IOB5 through 7 become Memory Pointer Access (MPA), End of Instruction (EOI), and DMA Acknowledge (DMA ACK) control signals, respectively, and are used for interfacing with external memories and devices. The lower four bits become the external DB where data is enabled onto the DB during READ, and transferred from DB during WRITE. The MPA control line, when activated, enables the contents of user registers to be read via software without disturbing the memory pointers P0 and P1 in the process. EOI (active low) signifies the completion of an instruction cycle. In this mode, DMA ACK is reassigned from its original position in normal mode to IOB7.

MAC-4 PIN DESCRIPTION (Cont.)

Input/Output Pins	Description
SERIN, SEROUT	Serial data can be transferred in (SERIN) or out (SEROUT) during DMA at a clock rate as provided by the $\overline{ASYN\ CLK}$ input.
IOL0 - 15	The 16 I/O latches can be individually designated as either inputs or outputs, and they are individually addressable. These latches are extremely useful as the outputs can serve as individual control lines or data bits to external devices, while the inputs can be individual input bit ports. As a user mask option, IOL12 through 15 are converted to provide "handshaking" signals (ODR, STBOUT, IBB, STBIN) so that IOB0 through 7 can be utilized in a bus structured environment. MAC-4 sets Output Data Ready (ODR) when data is available at IOB0 through 7; Strobe Out (STBOUT) strobes that data out and resets ODR. Input Buffer Busy (IBB) is set when data is strobed into IOB0 through 7 by Strobe In (STBIN) and is reset by MAC-4 when it reads that data into its memory. STBIN and STBOUT signals are initiated by the user. During the $\overline{EMA}$ mode: The 12-bit Address Bus, $\overline{AB0}$ through $\overline{AB11}$ (active low) appears at the lower 12 bits of IOL0 through 11 for External Memory Access by the processor. Data transfer is controlled by the $\overline{READ}$, WRITE strobes. The WRITE and $\overline{READ}$ strobes appear at IOL12, 14 allowing data to be transferred from and to the DB, respectively.
$\overline{DMA\ REQ}$	DMA Request input (active low). The appropriate DMA operation is initiated at the conclusion of a current instruction, according to the conditions of the I/O Control Register (IOCR). The operation ceases when the signal is removed. DMA is nonmaskable, and has a higher priority than Interrupt $(\overline{INTR})$.
$\overline{DMA\ ACK}/\overline{EMA}$	DMA Acknowledge output (active low) signal indicates that execution of the current instruction has been completed and that the processor is ready for full speed DMA. Applying an active-low signal to the $\overline{EMA}$ input forces the AB and the $\overline{READ}$, WRITE, and miscellaneous control lines to appear on the IOL and the IOB respectively. It also forces all program memory fetches to reference external memory. This is extremely useful for prototyping, debugging, testing, and program verification. In this mode, $\overline{DMA\ ACK}$ is reassigned to IOB7.
$\overline{INTR}$	Maskable interrupt input (active low). When enabled, an interrupt is initiated at the completion of a currently executing instruction. The interrupt is disabled after a RESET. $\overline{INTR}$ is of a lower priority than $\overline{DMA\ REQ}$.
$\overline{ASYN\ CLK}$	An externally generated asynchronous clock (active low) governs the rate of DMA transfer. Data is strobed in and out during DMA at the positive-going transition of the asynchronous clock. When enabled, it is also the input for the event counter.
Clock Pins	
CLKIN	Input for externally generated single-phase clock. A machine cycle frequency is the clock frequency divided by two. The maximum clock frequency is 3.58 MHz (TV crystal) at V_{DD} = 9V ± 1V, and the voltage swing of this clock source is V_{SS} to V_{DD}.
$\overline{XTAL}$	Connection to be used with CLKIN terminal for an external crystal if the on-chip oscillator is used. The crystal is connected between terminals CLKIN and $\overline{XTAL}$ in parallel to a resistance (10 megohms typical). Frequency trimming capacitors may be required at these terminals.*
CLKOUT/$\overline{RESET}$	The on-chip clock circuit divides the oscillator output by two to produce one timing pulse per machine cycle (CLKOUT). This signal may be used for the synchronization of external devices to MAC-4. Also used as an input for initializing the processor (active low), where the program counter and the IOCR are set to zero, and the interrupt and event counter enable conditions are cleared.

*A mask option may be available to provide RC timing.

MAC-4 INSTRUCTION SET

Instruction	Instruction Nibbles (See Note 1)								No. of Nibbles	Machine Cycles (2 Clock Cycles) (See Note 2)	
										4 Bit	8 Bit
PROGRAM TRANSFER											
Branch if Equal	1	MM	dn	sn	al	am			4-10	20	28
Branch if Not Equal	2	MM	dn	sn	al	am					
Branch if Less Than	0	MM	dn	sn	al	am					
Branch if Zero	5	Mx	dn	al	am				4-6	14	19
Branch if Not Zero	4	MM	dn	al	am						
Decrement Branch if Not Zero	8	Mx	dn	al	am						
†Branch if Bit Set	7	Mn	dn	al	am				4-6	13	–
†Branch if Bit Clear	6	Mn	dn	al	am						
†Branch	C	al	am						3	7	7
†Jump	E	al	C	am	ah				5	10	10
†Call	E	am	B	al	ah				5	18	18
†Short Call	B	am							2	14	14
†Return	E	O	F						3	13	13
Return Interrupt	E	O	E								
Jump if Equal	E	MM	1	dn	sn	al	am	ah	6-12	23	31
Jump if Not Equal	E	MM	0	dn	sn	al	am	ah			
Jump if Less Than	E	MM	0	dn	sn	al	am	ah			
Test Jump if Zero	E	MM	3	dn	sn	al	am	ah			
Jump if Zero	E	MM	5	dn	al	am	ah		6-8	17	22
Jump if Not Zero	E	MM	4	dn	al	am	ah				
Decrement Jump if Not Zero	E	Mx	8	dn	al	am	ah				
†Jump if Bit Set	E	Mn	7	dn	al	am	ah		6-8	17	–
†Jump if Bit Clear	E	Mn	6	dn	al	am	ah				
DYADIC											
Add	D	MM	8	dn	sn				3-9	19	27
Add with Carry	D	MM	9	dn	sn						
Subtract	D	MM	A	dn	sn						
Subtract with Borrow	D	MM	B	dn	sn						
And	D	MM	C	dn	sn						
Or	D	MM	D	dn	sn						
Exclusive Or	D	MM	E	dn	sn						
Move	3	MM	dn	sn					2-8	17	25
†Move Bit	D	MM	F	ba	dn	sn			4-10	20	–
MONADIC											
Increment	D	Mx	O	dn					3-5	13	18
Decrement	D	Mx	2	dn							
Complement	D	Mx	4	dn							
Set	D	Mx	6	dn							
Clear	D	Mx	5	dn							
Rotate Left through Carry	D	Mx	1	dn							
†Rotate Right through Carry	D	Mx	3	dn					3-5	13	–
†Set Bit	9	Mn	dn						2-4	11	–
†Clear Bit	A	Mn	dn								
MISCELLANEOUS											
†Halt	E	O	D						3	7	7
†XR Override	F	i							2	2	2

†Instructions not affected by Extension Register (XR) operand-width setting.

NOTES:

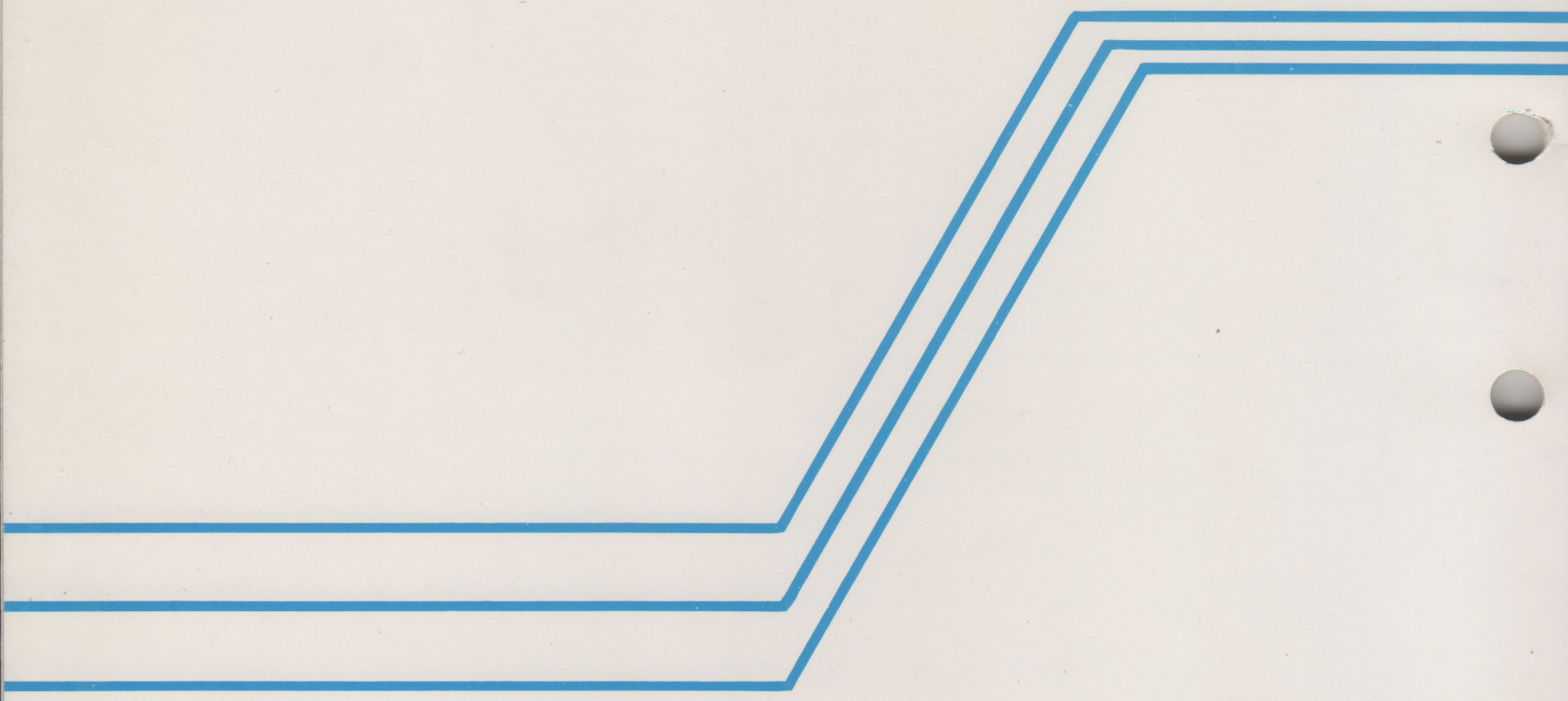
1. 0 through 9 and A through F = literal hexadecimal digit nibble.
   MM = destination (D) and Source (S) addressing modes as follows:

Mode	D	S
0	Indirect via group pointer	Indirect via group pointer
1	Direct address	Direct address
2	Indirect via memory pointer p0	Indirect via memory pointer p0
3	Indirect via memory pointer p1	Indirect via memory pointer p1

   Mn = destination mode and bit number
   Mx = destination mode in most significant 2 bits, zero in least significant 2 bits.
   dn and sn = destination address and source address, respectively. The number of nibbles used to form dn or sn depends on the addressing modes as follows:

Mode	dn	sn
0	dl	sl
1	dl dm	sl sm
2	none	none
3	none	i

   Where dl = low nibble of destination address.
   dm = middle nibble of destination address.
   sl = low nibble of source address.
   sm = middle nibble of source address.
   i = immediate data (which may range from 1 to 4 nibbles).

   al = low nibble of transfer address.
   am = middle nibble of transfer address.
   ah = high nibble of transfer address.
   ba = destination-nibble bit location and source-nibble bit location.

2. Machine cycles given for source addressing mode = 2, destination addressing mode = 2/3 only. Machine cycles vary for different combinations of addressing modes.